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(54) Three dimensional large storage random access memory device

(57) A random access memory device (300) includes one or more planes (200) of memory arrays (100) stacked on top of each other, each plane (200) being manufactured separately, and each array (100) with the plane (200) being enabled/disabled separately, thus enabling each memory array (100) to be individually tested. Memory planes (200) may be stacked on top of each other and on top of an active circuit plane (390) to make a large capacity memory device (300). The memory may be volatile or non-volatile by using appropriate memory cells (140) as base units. The memory plane (200) may be fabricated separately from the active circuitry and may be formed from a glass substrate. Each memory plane (200) may be individually selected (or enabled) via plane memory select transistors (240). The array (100) may be individually selected (or enable) via array select transistor (160). These transistors (160) may be formed from amorphous silicon transistor(s) and/or thin-film transistor(s). The data but (310), array select bus (330), and the plane select bus (340) provide electrical connections between the memory planes (200) and the active circuit plane (390) via side contact pads on each plane (200).

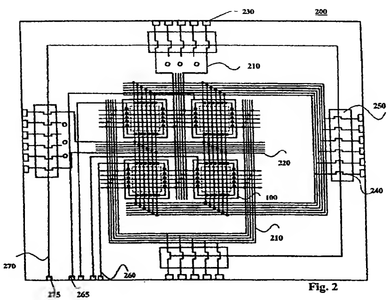

Fig. 2

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Description

[0001] This invention relates generally to memory devices. More particularly, the invention relates to 3-dimensional large storage random access memory devices.

[0002] The following patent applications contain related subject matter and are hereby incorporated by reference:

> European Patent Applications 02256632.7, 02256631.9, 02255452.1 and U.S. Patent Application Serial No. 09/924,500, entitled "ONE-TIME PROGRAMMABLE UNIT MEMORY CELL BASED ON VERTICALLY ORIENTED FUSE AND DIODE AND ONE-TIME PROGRAMMABLE MEMORY USING THE SAME" (Attorney Docket No. 10019168-1).

[0003] There is an ever-increasing demand for dense and large storage capacity in devices such as computers, communication equipments, consumer electronics, etc. This has led to great improvements in the storage and performance of data storage devices such as hard disk drives, solid-state memories, etc. In hard disk drives, small form factors in conjunction with great improvement in area density permitted development of high capacity disk drives.

[0004] In integrated circuits, the development of multichip modules (MCM) and hybrid manufacturing techniques have led to great reduction in size, and in some cases improved performance in the final product. A commonly used MCM configuration for the dynamic random access memories (DRAM) is the single-in-line memory modules (SIMM). Presently, many memory storage devices are limited to a single layer. This is due generally to two factors. First, active circuitry requires silicon as the base material to support the operation of the memory such as reading and writing. To read and write, address decoders, read/write control logic, sense amplifiers, output buffers, multiplexers, and more are included in a memory chip. These are generally referred to as overhead and typically consume 20-30 percent of the physical memory. Preferably, this overhead is kept low so more space is available for memory. Second factor limiting the memory storage device to a single array layer is the power dissipation constraints.

[0005] Recently, multiple array memories fabricated on top of complementary metal oxide semiconductor (CMOS) have been proposed. However, such approach requires via(s) for each memory layer so that each memory layer may be individually connected to the active circuitry. This approach may yield a very dense and efficient memory design for a few layers. But as number of layers increases, the number of via(s) increases to the point where it become difficult to route the signals from memory arrays to the CMOS layer and the routing paths become longer such that this design become less efficient, more complex, and the cost increases as well. The vias may be made small to overcome some of the problems. However, smaller vias correspondingly increase the risk of defects and increase the difficulty in alignment. In addition, interconnects between array layers becomes more difficult and complex.

[0006] In addition, the yield of the memory devices is relatively low. The low yield is due to the fact that an individual memory layer cannot be sorted and rejected from a stack of layers. To illustrate, if a single memory layer has a probability p(x) of being defective, then it is readily apparent that an MCM memory made of multiple layers has a probability greater than p(x) of having at least one defective layer. Because of the inability to sort and reject defects on an individualized memory layer level, the overall quality of the memory device suffers and, thus, the yield is low.

[0007] In one respect, an exemplary embodiment of a memory array may include a non-silicon based substrate. The memory array may also include a row conductor formed above the non-silicon based substrate and extending in a row direction and a column conductor formed above the non-silicon based substrate and extending in a column direction such that a cross-point is formed at an intersection between the row conductor and the column conductor. In the cross point, a memory cell may be formed. The memory array may further include an array enable circuit connected to enable/disable at least one of the row conductor and the column conductor.

[0008] In another respect, an exemplary embodiment of a memory plane may include a non-silicon based substrate and one or more memory arrays formed above the non-silicon based substrate. Each memory array may include a row conductor extending in a row direction and a column conductor extending in a column direction such that a cross-point is formed at an intersection between the row conductor and the column conductor. Each memory array may also include a memory cell formed in the cross-point, and an array enable circuit connected to enable/disable at least one of the row conductor and the column conductor.

[0009] In a further respect, an exemplary embodiment of a memory device may include an active circuit plane, for example CMOS circuit plane, and one or more memory planes formed above the active circuit plane. Each memory plane may include a non-silicon based substrate one or more memory arrays formed above the non-silicon substrate. Each memory array of each memory plane may include a row conductor extending in a row direction and a column conductor extending in a column direction such that a cross-point is formed at an intersection between the row conductor and the column conductor. Each memory array may also include a memory cell formed in the cross-point, and an array enable circuit connected to enable/disable at least one of the row conductor and the column conductor.

[0010] In yet another respect, an exemplary embodi-

ment of a method to fabricate a memory device may include forming an active circuit plane and forming one or more memory planes above the active circuit plane. The method may also include forming a non-silicon based substrate for each memory plane. For each memory plane, the may further include forming one or more memory arrays above the non-silicon substrate. In addition, for each memory array, the method may include forming a row conductor extending in a row direction and forming a column conductor extending in a column direction such that a cross-point is formed at an intersection between the row conductor and the column conductor. The method may still further include forming a memory cell in the cross-point and forming an array enable circuit connected to enable/disable at least one of the row conductor and the column conductor for each memory array.

[0011] The above-disclosed embodiments of the present invention may be capable of achieving certain aspects. For example, the memory device may be made with stacking multiple planes of memory arrays, with each plane being fabricated individually. This eliminates the need to fabricate vias and thus the relative complexity of the device is reduced. Also, each array may be individually enabled and disabled, for example through an array select line. Thus defective arrays and/or planes may be sorted out prior to completing the device, which results in increased yield and quality. Further, because the memory planes may be made separately from the active circuitry, substrates of the memory planes may be formed from materials other than silicon. Further yet, memory planes without including overheads such as read/write control logic, sense amplifiers, output buffers, and multiplexers may be fabricated, which increases the capacity by enabling more space to be dedicated to memory. Still further, stacking allows very high capacity to be achieved. In addition, the memory may be volatile, non-volatile, random access or one-time programmable.

[0012] Features and advantages of the invention will become apparent to those skilled in the art from the following description with reference to the drawings, in which:

Fig. 1A illustrates an exemplary embodiment of a memory array according to the principles of the invention;

Fig. 1B illustrates a second exemplary embodiment of a memory array according to the principles of the invention;

Fig. 2 illustrates an exemplary embodiment of a memory plane according to the principles of the invention;

Fig. 3 illustrates an exemplary embodiment of a memory device according to the principles of the invention; and

Fig. 4 is a flow chart representing an exemplary method to fabricate the memory device of Fig. 3 according to an aspect of the present invention.

[0013] For simplicity and illustrative purposes, the principles of the invention are described by referring mainly to exemplary embodiments thereof. However, one of ordinary skill in the art would readily recognize that the same principles are equally applicable to many types of solid-state memories and methods of fabricating and using thereof.

[0014] In accordance with the principles of the invention, fabricating multiple layers of memory arrays on top of one another may increase the capacity of a memory device. In an aspect of the invention, planes of memory arrays may be stacked to form a three-dimensional (3-D) memory device. Each plane may incorporate one or more memory arrays.

[0015] Fig. 1A illustrates an exemplary embodiment of a memory array 100 according to the principles of the invention. As shown in Fig. 1A, the memory array 100 may include a substrate 110. The substrate 110 may be silicon or non-silicon based. Examples of non-silicon based substrate include materials of plastic, glass, ceramics, non-metals such as electrical insulators, and the like.

[0016] Above the substrate 110, one or more row conductors 120 and one or more column conductors 130 may be formed. The row and column conductors 120 and 130 may extend in a row direction and column direction, respectively, to form a cross-point at each intersection. At a cross-point, a memory cell 140 may be formed. Each memory cell 140 may be individually addressable through the respective row and column conductors 120 and 130, respectively. The memory cell 140 may be read-only, randomly accessible, or one-time programmable, thus allowing the memory array 100 to be a read-only memory (ROM), random access memory (RAM), or one-time programmable memory (OTP), respectively. For example, the memory cell 140 may be a fuse memory cell, a fuse/diode memory cell, a fuse/antifuse memory cell, a magnetic memory cell, a diode memory cell, a magnetic/diode memory cell, a phase change memory cell, a resistive element cell, and the like.

[0017] The memory array 100 may also include an array enable circuit 170. The array enable circuit 170 may include one or more array enable transistors 160. For example, four groups of array enable transistors 160 are shown in Fig. 1A. Each row or column conductor, 120 or 130, respectively, may be connected to one or more array enable transistors 160. For example, as shown in Fig. 1A, each row or column conductor, 120 or 130, respectively, may be connected to two array enable transistors 160 on both ends. Conduction through the row conductor 120 or the column conductor 130 is enabled or disabled through controlling the array enable transistors 160. The array-enable transistors 160 may be formed from microcrystalline silicon transistors, amorphous silicon transistors, or any enable switches that do

not require silicon substrate.

[0018] The memory array 100 may further include an array select line 150 connected to the array-enable transistors 160. By controlling the signal to the array select line 150, the memory array 100 may be selected or disabled. Typically, in a multiple arrays setting, a single array line 150 is dedicated to one array 100 and is not shared with any other array 100.

[0019] Note that it's not necessary that both ends of the row or the column conductor 120 or 130 be connected to the array-enable transistor 160. Fig. 1B illustrates a second exemplary embodiment of a memory array according to the principles of the invention. As shown, only one of the ends of the row and column conductors, 120 and 130, respectively, are connected to the array enable transistors 160. Configurations other than Figs. 1A and 1B are possible without departing from the scope of the invention.

[0020] Regardless of whether the memory array 100 is silicon or non-silicon based, it is note worthy that the memory array need not include overhead such as sense amplifiers, output buffers, decoders, multiplexers, and the like. A single active circuitry layer may provide the memory location selections, sense amplifiers, and read and write controls.

[0021] While individual memory arrays 100 may be stacked to form a 3-D memory device, planes of memory arrays may be fabricated according to another aspect of the present invention. The planes of memory arrays then may be sorted and stacked to form a 3-D memory device, which relatively increases the storage capacity of the device.

[0022] Fig. 2 illustrates an exemplary embodiment of a memory plane 200 according to the principles of the invention. As shown in Fig. 2, the memory plane 200 may include one or more memory arrays 100, for example the memory arrays 100 of Figs. 1A and 1B, formed above the substrate 110 (not shown). Again, the substrate 110 may be silicon or non-silicon based. The memory plane 200 may also include one or more row buses 210 and one or more column buses 220. The row buses 210 may electrically connect to the row conductors 120 (not labeled) of the memory arrays 100. Similarly, the column buses 220 may electrically to the column conductors 130 (also not labeled) of the memory arrays 100. Through the row and column buses 210 and 220, an individual memory cell 140 (not shown in Fig. 2) of individual memory arrays 100 may be addressed.

[0023] The memory plane 200 may further include a plane enable circuit 250. The plane enable circuit 250 may include one or more plane-enable transistors 240. For example, four groups of plane-enable transistors 240 are shown in Fig. 2. Data flow to and from the row and column buses, 210 and 220, and consequently from the memory cells 140 (not shown in Fig. 2) of the memory arrays 100 may be enabled or disabled through controlling the plane enable transistors 240. The plane-enable transistor 240 may be formed from microcrystalline thin-film transistor, amorphous thin-film transistor, or any enable switch that do not require silicon substrate.

[0024] A plane select line 270 may be included in the memory plane 200, in which the plane select line 270 is connected to the plane enable transistors 240. In this manner, by controlling the signal to the plane select line 270, the memory plane 200 may be enabled or disabled.

[0025] The memory plane 200 may yet further include one or more data side contact pads 230. The data side contact pads 230 may electrically connect with the row and column buses, 210 and 220, via the plane enable transistors 240. The memory plane 200 may be fabricated so that when multiple memory planes 200 are stacked, the data side contact pads 230 of the memory planes 200 are aligned for the next conductor process step to form data buses 310 (see Fig. 3). In this manner, the need to fabricate the interconnect vias between planes may be eliminated and the relative complexity of the device may be reduced.

[0026] Note that the array select line 150 of individual memory arrays 100 may come together to form a plurality of array select lines 260. The memory plane 200 and the active circuit plane 390 may be fabricated so that when multiple memory planes 200 are stacked together, the data side contact pads 230 are aligned that ease the interconnection of multiple memory planes and the active circuit plane. A deposition, plating or screening conductor process step may be used for the interconnections and to form array select bus 330 (see Fig. 3). Since the conductors of the array select bus 330 are physically wide, this process is easily accomplished.

[0027] Fig. 3 illustrates an exemplary embodiment of a memory device 300 according to the principles of the invention. As shown, the memory device 300 may include one or more memory planes 200 stacked to form a 3-D memory. The memory device 300 may also include an active circuit plane 390. The active circuit plane 390 may be built on a silicon substrate and may contain circuits necessary to address the memory arrays 100 of memory planes 200 including overhead elements such as address decoders, read/write control logic, sense amplifiers, output buffers, multiplexers.

[0028] The memory device 300 may further include one or more data buses 310. The data buses 310 may be formed from a conductor process step to connect the aligned data side contact pads 230 (see Fig. 2) of the memory planes 200. Note that the active circuit plane 390 may also include data side contact pads that are aligned and electrically connected to the data side contact pads 230 of the memory planes 200 as well.

[0029] The memory device 300 may still further include the array select bus 330. The array select bus 330 may be formed from a conductor process that connect electrically the plurality of array select lines 260 through the array select side contact pads 265 on the memory planes 200 and the array select side contact pads on the active plane 390. Note that the active circuit plane 390 may also include array select lines and array select

side contact pads that aligned with the array select side contact pad 265 of the memory planes 200 as well.

[0030] The memory device 300 may include a plane select bus 340. The plane select bus 340 may be formed from combination of the plane select lines 270 and a plane select side contact pad 275 (see Fig. 2) of individual memory planes. A conductor process step interconnects electrically the plane select lines 270 via the plane select side contact pad 275 on the individual memory planes 200 to the active circuit plane 390. Each plane 200 may have a separate plane select line 270, but the array select bus 330 may shared among the planes 200.

[0031] Fig. 4 is a flow chart representing an exemplary method 400 to fabricate the memory device 300 of Fig. 3 according to an aspect of the present invention. As shown in Fig. 4, the active circuit plane 390 may be fabricated (step 410). Also, one or more memory planes 210 may be fabricated (steps 420 and 430). Note that fabricating the active circuit plane 390 may take place before, after, or simultaneously with fabricating the memory planes 200.

[0032] Then, the memory planes 200 may be sorted according to a predetermined error threshold (step 440). For example, a threshold may be set to reject any memory plane 200 with more than 10% of the memory arrays 100 being defective. Thus if each memory plane 200 has sixteen memory arrays 100, then a plane 200 with more than one defective array 100 will be rejected. Such control assures that the resulting device meets a preset tolerance for defects. To sort out bad a memory plane, a tester or an electronics assembly that have read/write and control functions similar to the active circuit plane may be used. The screening step 440 is done at wafer probe testing stage before the wafers are diced into individual planes 200. A wafer may contain several planes 200.

[0033] Indeed, multiple threshold levels may be used to sort the memory planes 200. For example, it may be possible that certain applications may be able to tolerate more defects than others. In this manner, varying defect tolerance levels can be assured in the memory devices.

[0034] Then to complete the process, the active circuit plane 390 and the memory planes 200 may be stacked and bonded with adhesive material to hold them together. The stacking process also aligned the side contact pads (data 230, array select 265, and plane select 275) of the memory planes 200 and the active circuit planes 390. The conductor process forms the plane interconnect conductors 310, 330, and 340 to make electrical connections between memory planes and the active circuit plane. The memory stacks are then sent through a packaging process to form the memory device 300.

[0035] While the invention has been described with reference to the exemplary embodiments thereof, those skilled in the art will be able to make various modifications to the described embodiments of the invention without departing from the true spirit and scope of the invention. For example, the terms "row" and "column" are merely relative, and do not imply any fixed orientation. Also, "rows" and "columns" are interchangeable, in that others may refer to "rows" what this document calls columns and vice versa. The terms "row" and "column" do not necessarily imply an orthogonal relationship, although that is what has been illustrated herein. The terms and descriptions used herein are set forth by way of illustration only and are not meant as limitations. In particular, although the method of the invention has been described by examples, the steps of the method may be performed in a different order than illustrated or simultaneously. Those skilled in the art will recognize that these and other variations are possible within the scope of the invention as defined in the following claims and their equivalents.

Claims

1. A memory plane (200), comprising:

   a substrate (110);
   a plurality of array select lines (150) formed above said substrate (110);
   a plane-enable circuit (250) formed above said substrate (110) and configured to enable/disable said memory plane (200);
   a plane select line (270) electrically connected to said plane-enable circuit (250); and
   one or more memory arrays (100) formed above said substrate (110), wherein at least one memory array (100) includes:

      one or more row conductors (120) formed above said substrate (110) and extending in a row direction;
      one or more column conductors (130) formed above said substrate (110) and extending in a column direction such that a cross-point is formed at each intersection between said row (120) and column conductors (130);
      a memory cell (140) formed in one or more of said cross-points; and
      an array-enable circuit (170) configured to enable/disable said memory array (100) and electrically connected at least one of said plurality of array select lines (150).

2. The memory plane (200) of claim 1, further comprising:

   a row bus (210) electrically connected to said one or more row conductors (120) of said one or more memory arrays; and
   a column bus (220) electrically connected to said one or more column conductors (130) of said one or more memory arrays (100).

3. The memory plane (200) of claim 1, wherein said substrate (110) is silicon based and wherein each of said one or memory arrays (100) excludes sense amplifiers, output buffers, decoders, and multiplexers.

4. The memory plane (200) of claim 1, wherein said substrate (110) is non-silicon based and is formed from base materials of at least one of a plastic, glass, ceramic, and non-metal.

5. The memory plane (200) of claim 1, wherein said memory cell (140) includes at least one of a fuse memory cell, a fuse/diode memory cell, a fuse/antifuse memory cell, a magnetic memory cell, a diode memory cell, a magnetic/diode memory cell, a phase change memory cell, and a resistive element cell.

6. A memory device (300), comprising:

an active circuit plane (390);
a data bus (310) electrically connected to said active circuit plane (390);
a plane select bus (340) electrically connected to said active circuit plane (390);
an array select bus (330) electrically connected to said active circuit plane (390); and
one or more memory plane (200)s stacked above said active circuit plane (390), wherein at least one memory plane (200) includes:

a substrate (110);
a plurality of array select lines (150) formed above said substrate (110) and electrically connected to said array select bus (330);
a plane-enable circuit (250) configured to enable/disable said memory plane (200);
a plane select line (270) electrically connected to said plane enable-circuit (250) and to said plane select bus (340); and
one or more memory arrays (100) formed above said substrate (110), wherein at least one memory array (100) includes:

one or more row conductors (120) formed above said substrate (110) and extending in a row direction;
one or more column conductors (130) formed above said substrate (110) and extending in a column direction such that a cross-point is formed at each intersection between said row and column conductors;
a memory cell (140) formed in one or more of said cross-points; and
an array-enable circuit (170) configured to enable/disable said memory array (100) and electrically connected at least one of said plurality of array select lines (150).

7. The memory device (300) of claim 6, wherein said at least one memory plane (200) further comprises:

a row bus (210) electrically connected to said one or more row conductors (120)of said one or more memory arrays; and
a column bus (220) electrically connected to said one or more column conductors (130)of said one or more memory arrays.

8. The memory device (300) of claim 7, wherein said at least one memory plane (200) further comprises at least one of:

a plurality of data side contact pads (310) electrically connected to said row (210) and column (220) buses;
a plurality of array select side contact pads (330) electrically connected to said array select lines (150); and
a plane select side contact pad (340)n electrically connected to said plane select line (270).

9. The memory device (300) of claim 8, wherein at least one of:

said plurality of data side contact buses (310) are aligned and electrically connect to said data bus (310);
said plurality array select side contact pads (330) are aligned and electrically connect to said array select bus (330); and
said plane select side contact pad (340) electrically connects with a line of said plane select bus (340).

10. The memory device (300) of claim 6, wherein said plurality of array select lines (150) of said memory plane (200)s are electrically connected to from said array select bus (330).

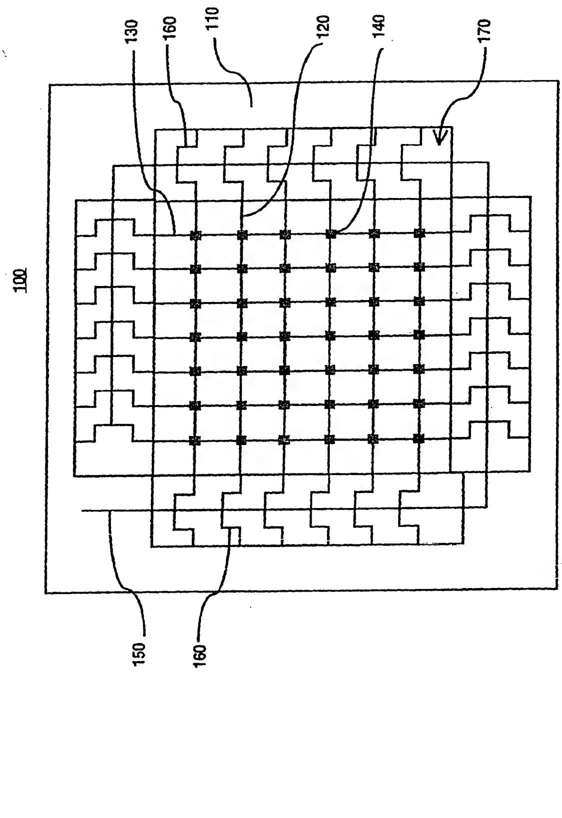

FIG. 1A

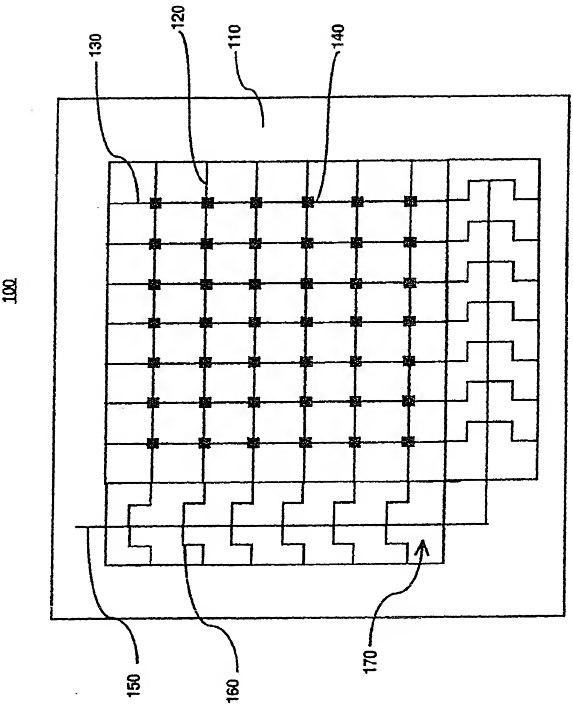

FIG. 1B

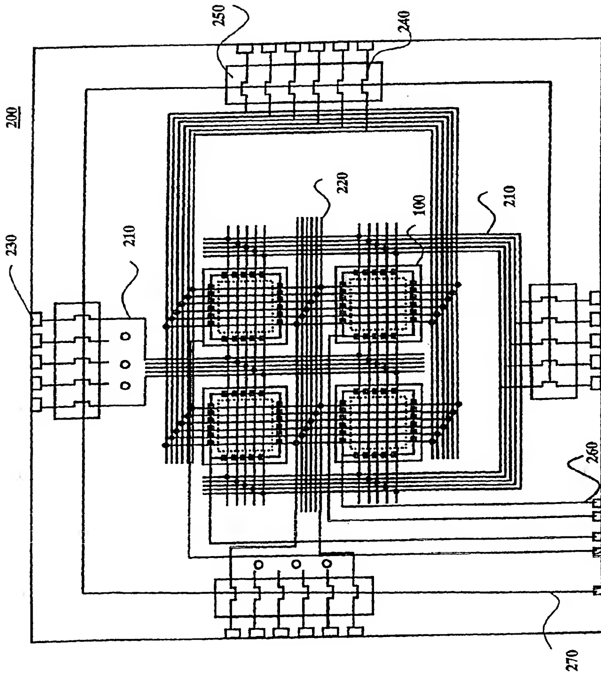

Fig. 2

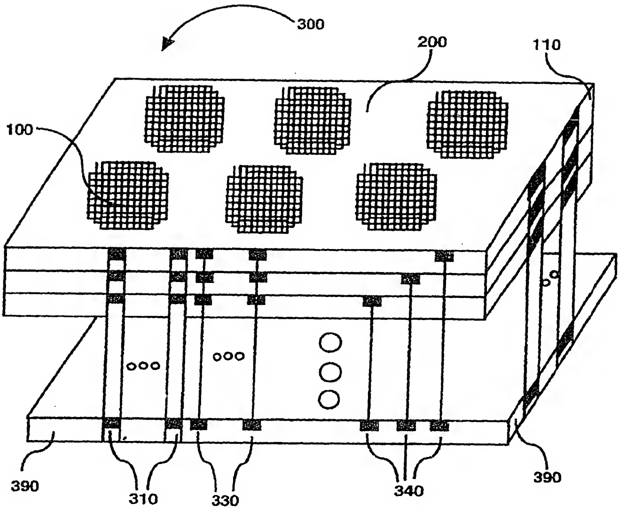

FIG. 3

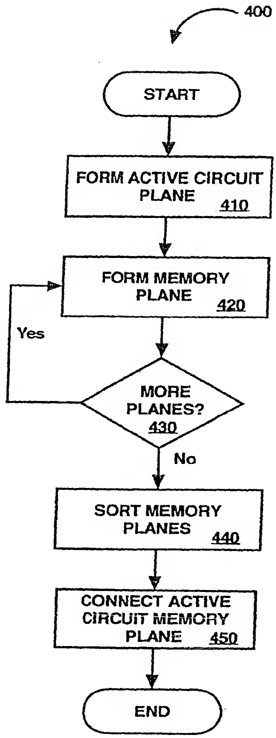
400
START
FORM ACTIVE CIRCUIT PLANE 410
FORM MEMORY PLANE 420
Yes
MORE PLANES? 430
No
SORT MEMORY PLANES 440
CONNECT ACTIVE CIRCUIT MEMORY PLANE 450
END

FIG. 4

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(54) **Three dimensional large storage random access memory device**

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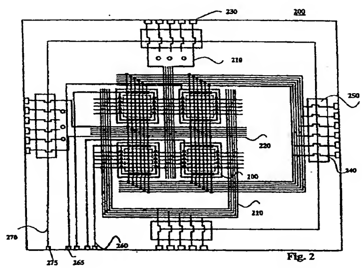

Fig. 2

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 25 7425

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Y	EP 1 017 100 A (SEIKO EPSON CORP) 5 July 2000 (2000-07-05) * figure 21 * * figure 26 * * paragraph [0118] - paragraph [0128] * * paragraph [0155] - paragraph [0172] * * paragraph [0187] * ---	1-10	G11C8/12 H01L21/822 H01L25/065
X Y	US 6 236 594 B1 (KWON SEOK-CHEON) 22 May 2001 (2001-05-22) * figure 2 * ---	1,2,5 1-10	
Y	WO 99 63527 A (GUDESEN HANS GUDE ;LEISTAD GEIRR I (NO); NORDAL PER ERIK (NO); OPT) 9 December 1999 (1999-12-09) * figure 4 * * page 7 * * page 10 - page 11 * ---	8,9	
A	WO 95 09438 A (KOPIN CORP) 6 April 1995 (1995-04-06) * figure 14 * ---	1-10	TECHNICAL FIELDS SEARCHED (Int.Cl.7)
A	US 5 786 629 A (FARIS SADEG MUSTAFA) 28 July 1998 (1998-07-28) * figure 6 * * abstract * -----	1-10	G11C H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	7 March 2003	Havard, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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D : document cited in the application
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